REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow. Claims 1-20 are pending in the present application, with Claims 5 and 13-16 having been previously withdrawn from consideration. Claims 1-4, 6-12, and 17-20 were rejected by the Examiner. Claims 1, 9, and 17 have been amended. No new matter has been added. Accordingly, Claims 1-20 will remain pending in the present application upon entry of this Amendment and Reply.

A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

Priority

On page 2 of the Office Action, the Examiner indicates that the present application claims priority to U.S. Patent Application No. 10/341,683, and requests that the Applicant file necessary papers to correct this error.

As noted in the Preliminary Amendment filed on May 10, 2004 by the Applicant, this is a typographical error included in the original patent application paperwork. The Preliminary Amendment included an amendment of paragraph [0001] to correct the typographical error such that the present application claims priority to U.S. Patent Application No. 10/341,863. A Supplemental Application Data Sheet and Request for Corrected Filing Receipt was also filed concurrently therewith. Such documents are available in the USPTO PAIR system for the Examiner's reference.

Double Patenting

On pages 3-4 of the Office Action, the Examiner objected various claims under the judicially-created doctrine of obviousness-type double patenting. Specifically, Claims 1-3 and 9-11 were rejected as being unpatentable over Claims 1-3 and 9-11 of U.S. Patent No. 6,673,696; Claims 1-3 and 9-11 were rejected as being unpatentable over Claims 1-3 and 9-11 of U.S. Patent No. 6,292,857; and Claims 1-3, 9-11, and 17-18 were rejected as being

unpatentable over Claims 21-23, 28-30, and 36-37 of copending U.S. Patent Application No. 10/389,456.

The Applicants request that the double patenting rejections described on pages 3-4 of the Office Action be held in abeyance until allowable independent claims are indicated by the Examiner in the present Application (since a timely filed terminal disclaimer would overcome the rejection such that further consideration of the claims on that rejection should not be necessary). 37 C.F.R. § 1.111(b).

Claim Rejections – 35 U.S.C. § 102

On page 4 of the Office Action, the Examiner rejected Claims 1-2, 6, 8, and 17-18 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,266,813 to Comfort et al. The Applicant respectfully traverses this rejection.

Claim 1 (as amended) is in independent form and recites a "method of manufacturing an integrated circuit" comprising, in combination with other elements, "providing a semiconductor or metal layer by selective epitaxial growth directly in contact with the sidewalls such that the semiconductor or metal layer is in direct contact with the silicon-germanium layer and the strained silicon layer; and converting the semiconductor or metal layer in the trenches of the substrate into oxide liners."

Claim 17 (as amended) is in independent form and recites a "method of forming a liner in a trench" comprising, in combination with other elements, "providing a semiconductor layer in the trench by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer; and converting the semiconductor layer into an oxide liner such that substantially all of the semiconductor layer is consumed during the conversion."

Comfort et al. does not identically disclose "converting a semiconductor or metal layer in the trenches of the substrate into oxide liners" as recited in independent Claim 1 or "converting a semiconductor layer into an oxide liner such that substantially all of the semiconductor layer is consumed during the conversion" as recited in independent Claim 1.

In contrast, Comfort et al. discloses that an "epitaxial layer of silicon is deposited both in the trench and on the surface of the pad layer 40" (column 5, lines 11-12), after which a "silicon dioxide layer 70 is formed over the single crystal silicon layers 50 and 60" (column 5, lines 36-37). Thus, rather than converting layer 60 into silicon dioxide to form an oxide liner, an entirely separate layer of material is provided over the "epitaxial layer of silicon," as illustrated in Figure 3 of Comfort et al.

The Applicants respectfully request withdrawal of the rejection of Claims 1-2, 6, 8, and 17-18 under 35 U.S.C. § 102(b), because at least one limitation of independent Claims 1 and 17 are not identically disclosed by Comfort et al.

Claim Rejections – 35 U.S.C. § 103

1. Claims 1-3 and 6-8

On page 6 of the Office Action, Claims 1-3 and 6-8 were rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,136,664 to Economikos et al. in view of an article to Van Zant. Applicant respectfully traverses this rejection.

Claim 1 (as amended) is in independent form and recites a "method of manufacturing an integrated circuit" comprising, in combination with other elements, "providing a semiconductor or metal layer by selective epitaxial growth directly in contact with the sidewalls such that the semiconductor or metal layer is in direct contact with the silicon-germanium layer and the strained silicon layer; and converting the semiconductor or metal layer in the trenches of the substrate into oxide liners."

Economikos et al., either alone or in proper combination with Van Zant, does not teach or suggest "providing a semiconductor or metal layer by selective epitaxial growth directly in contact with the sidewalls" of a trench "such that the semiconductor or metal layer is in direct contact with the silicon-germanium layer and the strained silicon layer."

In contrast, Economikos et al. discloses that a "thin layer of silicon nitride 50 is deposited" in the "trench 47," after which "a layer of polycrystalline silicon or amorphous silicon 60 is deposited on the surface by low pressure chemical vapor deposition" (column 4,

lines 14-22; Figure 2D). Accordingly, Economikos et al. does not teach or suggest that the "layer of polycrystalline silicon or amorphous silicon 60" is in direct contact with the sidewalls of the trench; instead, an intervening "silicon nitride layer 50" is provided between the layer 60 and the sidewalls.

The rejection of Claims 1-3 and 6-8 should be withdrawn, because at least one limitation of independent Claim 1 (and corresponding dependent Claims 2-3 and 6-8) is not taught or suggested by Economikos et al., either alone or in proper combination with Van Zant. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 1-3 and 6-8 under 35 U.S.C. § 103(a).

2. Claims 9-11 and 17

On page 8 of the Office Action, Claims 9-11 and 17 were rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,136,664 to Economikos et al. in view of an article to Van Zant and U.S. Patent No. 5,700,712 to Schwalke. Applicant respectfully traverses this rejection.

Claim 9 (as amended) is in independent form and recites a "method of forming shallow trench isolation regions in a strained semiconductor layer" comprising, in combination with other elements, "providing a conformal semiconductor layer in the trenches in direct contact with the strained semiconductor layer by selective epitaxial growth; and oxidizing the conformal semiconductor layer to form a liner in the trenches."

Claim 17 (as amended) is in independent form and recites a "method of forming a liner in a trench" comprising, in combination with other elements, "providing a semiconductor layer in the trench by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer; and converting the semiconductor layer into an oxide liner such that substantially all of the semiconductor layer is consumed during the conversion."

None of the cited references, whether taken alone or in proper combination, teach or suggest "providing a conformal semiconductor layer in the trenches in direct contact with" a "strained semiconductor layer" (Claim 9) or "providing a semiconductor layer in the trench

by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer" (Claim 17).

For example, neither Economikos et al. nor Schwalke teach or suggest a "strained" layer (e.g., a strained semiconductor layer) or a "germanium containing layer." For example, Schwalke discloses a "monocrystalline silicon layer 3" and Economikos et al. discloses a "silicon substrate."

Even if it were true that Van Zant provides "art recognized equivalence" between silicon substrates and silicon-germanium substrates (and the Applicant submits that there is no such art-recognized equivalence), none of the cited references teach or suggest a strained layer such as a strained semiconductor layer. One exemplary embodiment of such a strained layer is described, for example, at paragraphs [0038] and [0042]-[0043] of the present specification.

The rejection of Claims 9-11 and 17 should be withdrawn, because at least one limitation of independent Claims 9 and 17 (and corresponding dependent Claims 10-11) is not taught or suggested by Economikos et al., Van Zant, and Schwalke, either alone or in proper combination. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 9-11 and 17 under 35 U.S.C. § 103(a).

3. Claims 18 and 19

On pages 10 and 13 of the Office Action, Claims 18 and 19 were rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,136,664 to Economikos et al. in view of an article to Van Zant, U.S. Patent No. 5,700,712 to Schwalke, and an article by Vossen et al. Applicant respectfully traverses these rejections.

Claim 17 (as amended) is in independent form and recites a "method of forming a liner in a trench" comprising, in combination with other elements, "providing a semiconductor layer in the trench by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer; and converting the semiconductor layer into an oxide liner such that substantially all of the semiconductor layer is consumed during the conversion."

As described above, the combination of Economikos et al., Van Zant, and Schwalke does not teach or suggest "providing a semiconductor layer in the trench by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer." Vossen et al., whether taken alone or in combination with Economikos et al., Van Zant, and Schwalke, also does not provide such a teaching or suggestion.

The rejection of Claims 18-19 should be withdrawn, because at least one limitation of independent Claim 17 (and corresponding dependent Claims 18-19) is not taught or suggested by Economikos et al., Van Zant, Schwalke, and Vossen et al., either alone or in proper combination. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 18-19 under 35 U.S.C. § 103(a).

4. Claim 20

On page 11 of the Office Action, Claim 20 was rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,136,664 to Economikos et al. in view of an article to Van Zant, U.S. Patent No. 5,700,712 to Schwalke, and U.S. Patent No. 6,146,970 to Witek et al. Applicant respectfully traverses this rejection.

Claim 17 (as amended) is in independent form and recites a "method of forming a liner in a trench" comprising, in combination with other elements, "providing a semiconductor layer in the trench by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer; and converting the semiconductor layer into an oxide liner such that substantially all of the semiconductor layer is consumed during the conversion."

As described above, the combination of Economikos et al., Van Zant, and Schwalke does not teach or suggest "providing a semiconductor layer in the trench by selective epitaxial growth such that the semiconductor layer is in direct contact with the germanium containing layer and the strained layer." Witek et al., whether taken alone or in combination with Economikos et al., Van Zant, and Schwalke, also does not provide such a teaching or suggestion.

The rejection of Claim 20 should be withdrawn, because at least one limitation of independent Claim 17 (and corresponding dependent Claim 20) is not taught or suggested by Economikos et al., Van Zant, Schwalke, and Witek et al., either alone or in proper combination. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claim 20 under 35 U.S.C. § 103(a).

5. Claim 4

On page 11 of the Office Action, Claim 4 was rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,136,664 to Economikos et al. in view of an article to Van Zant and U.S. Patent No. 6,146,970 to Witek et al. Applicant respectfully traverses this rejection.

Claim 1 (as amended) is in independent form and recites a "method of manufacturing an integrated circuit" comprising, in combination with other elements, "providing a semiconductor or metal layer by selective epitaxial growth directly in contact with the sidewalls such that the semiconductor or metal layer is in direct contact with the silicon-germanium layer and the strained silicon layer; and converting the semiconductor or metal layer in the trenches of the substrate into oxide liners."

The combination of Economikos et al., Van Zant, and Witek et al. does not teach or suggest "providing a semiconductor or metal layer by selective epitaxial growth directly in contact with the sidewalls such that the semiconductor or metal layer is in direct contact with the silicon-germanium layer and the strained silicon layer."

The rejection of Claim 4 should be withdrawn, because at least one limitation of independent Claim 1 (and corresponding dependent Claim 4) is not taught or suggested by Economikos et al., Van Zant, and Witek et al., either alone or in proper combination. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claim 4 under 35 U.S.C. § 103(a).

6. Claim 12

On page 12 of the Office Action, Claim 12 was rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,136,664 to Economikos et al. in view of an article to Van Zant, U.S. Patent No. 5,700,712 to Schwalke, and GB 2254731 to Cho et al. Applicant respectfully traverses this rejection.

Claim 9 (as amended) is in independent form and recites a "method of forming shallow trench isolation regions in a strained semiconductor layer" comprising, in combination with other elements, "providing a conformal semiconductor layer in the trenches in direct contact with the strained semiconductor layer by selective epitaxial growth; and oxidizing the conformal semiconductor layer to form a liner in the trenches."

The combination of Economikos et al., Van Zant, Schwalke, and Cho et al. does not teach or suggest "providing a conformal semiconductor layer in the trenches in direct contact with the strained semiconductor layer by selective epitaxial growth."

The rejection of Claim 12 should be withdrawn, because at least one limitation of independent Claim 9 (and corresponding dependent Claim 12) is not taught or suggested by Economikos et al., Van Zant, Schwalke, and Cho et al., either alone or in proper combination. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claim 12 under 35 U.S.C. § 103(a).

* * *

It is submitted that each outstanding objection and rejection to the Application has been overcome, and that the Application is in a condition for allowance. The Applicant requests consideration and allowance of all pending claims.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment,

to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 5/22/2006 By _____

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